

REMARKS

Claims 1-16 are all the claims pending in the application.

I. Claim Rejections—35 USC §103

The Examiner rejected claims 1, 5, 8, 9, 10, 13 and 14 under 35 USC §103(a) as allegedly being unpatentable over Nong (US 2003/0123468 A1). The Applicant respectfully traverses this rejection.

Claim 1

The Applicant submits that Nong does not make the invention of claim 1 obvious, as Nong not only fails to teach a “memory unit organized as a number of physical memory queues, each queue being assigned to an output port,” but Nong actually teaches *away* from the claimed invention. The Examiner admits that Nong fails to disclose a single memory unit organized as a number of physical queues, but argues that it would have been obvious to one of ordinary skill in the art when the invention was made “to consider the input port (out of a plurality of input ports) of Nong as the memory unit comprising a number of data buffers for assigning data in specific input queues to be routed to specific output queues.” However, the input port of Nong still does not disclose or provide any motivation for a memory unit organized as a number of physical memory queues, as disclosed in claim 1. Nong does not disclose the use of a

single input port with a single “memory unit” of data buffers, but rather the use of multiple input ports with multiple data buffers to receive data, as is typical of a complex network node or switch. Figures 3, 4 and 5 of Nong actually illustrate a packet switch organized *completely the opposite* of the memory unit disclosed in claim 1.

First, Figure 3 illustrates how multiple input ports 210A-C feed different output ports 220A-C using multiple different buffers B11-Bnn within the switch fabric. The buffers are not organized as a single memory unit with a number of *physical* memory queues, with each queue assigned to an output port, as packets from a single input port will end up passing through multiple different buffers and sent to multiple different output ports. For example, packets from Input Port 1 210A are passed to Buffers B11, B12, etc. The packets at Buffer B11 are then passed to Output Port 1 220A while the packets from Buffer B12 are passed to Output Port 2 220B. In contrast, the invention of claim 1, as illustrated in Fig. 2 of the Application, sends all data through a single memory queue 22 that is then output to a specific output port 25. While Nong sends data to multiple different memory buffers and multiple different output ports, the invention of claim 1 aligns memory queues so that data passes through a single memory queue and is output to a single output port.

Further, Nong provides no teaching, suggestion or motivation for a memory unit organized as a number of physical memory queues, as stated in claim 1. As stated in the Specification, “the present invention really aligns queues *physically* in concrete memory blocks of a compact memory module towards single outputs...” *Specification*, p. 5, first paragraph (emphasis added). Nong discloses no such structure where a single memory unit is organized into a number of physical memory queues. In fact, Figures 4 and 5 of Nong *teach away* from the claimed invention, as they distribute memory buffers outward to different input ports and output ports instead of keeping them centralized in the switch fabric 230 of Figure 3. Again, Figure 5 illustrates how data in one input port is fed through multiple different buffers and sent to multiple different output ports. Figure 4 similarly feeds data from multiple different input ports to multiple different buffers in multiple different output ports. To combine the buffers into a physical memory unit and align them into queues, where each queue feeds data to a specific output port, is *completely in opposition* to the teaching in Nong. Nong attempts to divide the buffers out to different input ports and output ports, while the invention of claim 1 centralizes the memory queues into a single memory unit. Therefore, Nong actually teaches away from the invention of claim 1.

For at least the reasons stated above, the Applicant submits that it is not obvious from the teachings of Nong to arrive at the invention of claim 1, wherein memory units are organized into a number of physical memory queues, each queue being assigned to an output port. The Applicant therefore respectfully requests that the Examiner withdraw the rejection under 35 USC §103(a).

Claims 2-16

The Applicant further submits that claims 2-13 and 16 are allowable at least based on their dependency to claim 1. Further, the Applicant submits that the arguments presented above with regard to claim 1 are additionally applicable to the elements of the method of claims 14 and 15, and submits that Nong similarly fails to make the elements of claims 14 and 15 obvious as required by 35 USC §103(a).

Claim 5

The Applicant also submits that Nong fails to disclose where “each memory queue is assigned to a memory agent controlling the operation of the memory queue,” as stated in claim 5. The Examiner cites to Figure 8 and 9 of Nong, which only disclose a single buffer manager 815, 910, respectively, to control the multiple the operations of the buffers. In contrast, the Specification of the claimed invention states that “[t]he queuing agent 70 is assigned to a single memory queue 22, i.e. *a memory device 11*

comprises a number of such queuing agents 70 corresponding to the number of memory queues 22." *Specification*, p. 14, second paragraph (emphasis added). The invention of claim 5 discloses where each memory queue is assigned to a memory agent. Nong does not disclose more than a single buffer manager for controlling the plurality of buffers. Therefore, Nong does not disclose the elements of claim 5.

Claim 3

The Examiner rejected claim 3 under 35 USC §103(a) as allegedly being unpatentable over Nong in view of Bohm et al (US 2002/0027816 A1) as applied to claim 2, and in further view of Strehler (US 5,122,984).

The Applicant submits that neither Bohm nor Strehler provide any motivation to combine with the elements of Nong to teach the invention of claim 3. Further, the Examiner has failed to provide any apparent reason or rationale for combining the elements of Bohm, Strehler and Nong to arrive at the invention of claim 3. Bohm and Strehler are directed simply to memory systems for organizing memory units, but provide no motivation to combine the system into a network node or even a packet-switching application such as Nong. Nong, as admitted by the Examiner, does not teach a single memory unit as in the invention of claim 3. Therefore, there is no teaching, suggestion or motivation in Nong, Bohm or Strehler for the invention of claim

3, where a memory unit organized as a number of physical memory queues can re-distribute memory cells between memory queues.

II. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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